# NIHAL NAVAS

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## SUMMARY

*VLSI engineering graduate with strong fundamentals in **RTL design, Verilog/SystemVerilog, digital logic, and ASIC design flow**. Hands-on experience with **functional verification, STA, and synthesis** using tools such as **ModelSim, Design Compiler, and Vivado**. Seeking an entry-level role as a **VLSI / RTL / Verification Engineer**.*

## SKILLS

**HDL:** Verilog, SystemVerilog
**Programming:** C, C++, Python, Shell Scripting
**Digital Design:** Combinational & Sequential Logic, FSM Design, Timing Analysis
**VLSI Concepts:** CMOS Basics, STA, Setup & Hold Analysis, Power Analysis
**Verification:** Testbench Development, Functional Verification, Simulation, Debugging
**EDA Tools:** ModelSim, Xilinx Vivado, Synopsys Design Compiler (Basics), Cadence Virtuoso
**FPGA:** RTL Coding, Synthesis, Implementation, Bitstream Generation
**Physical Design (Basics):** Floorplanning, Placement, CTS, Routing, Timing Closure
**OS:** Linux, Windows
**Soft Skills:** Problem Solving, Debugging, Documentation

## PROJECT EXPERIENCE

### RTL Design & Verification of UART Communication Protocol [Project Link]

- *Designed UART TX/RX supporting configurable baud rate with FSM based architecture.*
- *Developed self-checking SystemVerilog testbench achieving 100% functional coverage.*
- *Verified framing errors, parity, baud mismatch scenarios using constrained random testing.*

*Tools & Technologies: Verilog, SystemVerilog, ModelSim, Xilinx Vivado, RTL Simulation, Testbench*
*Training Institute: IIES Bangalore*

### FPGA Implementation of 4-Bit ALU with Timing Analysis [Project Link]

- *Designed synthesizable Verilog ALU with arithmetic and logical operations.*
- *Achieved timing closure with zero setup violations after STA optimization.*
- *Generated FPGA bitstream and validated functionality on hardware.*

*Tools & Technologies: Verilog, Xilinx Vivado, RTL Synthesis, FPGA Implementation,*
*Training Institute: IIES Bangalore*

## EDUCATION

**B.E – ECE** Vinayaka Mission Research Foundation **2020-2024**

## TRAINING/CERTIFICATIONS

**VLSI Design** *IIES Bangalore* **2025 - 2026**